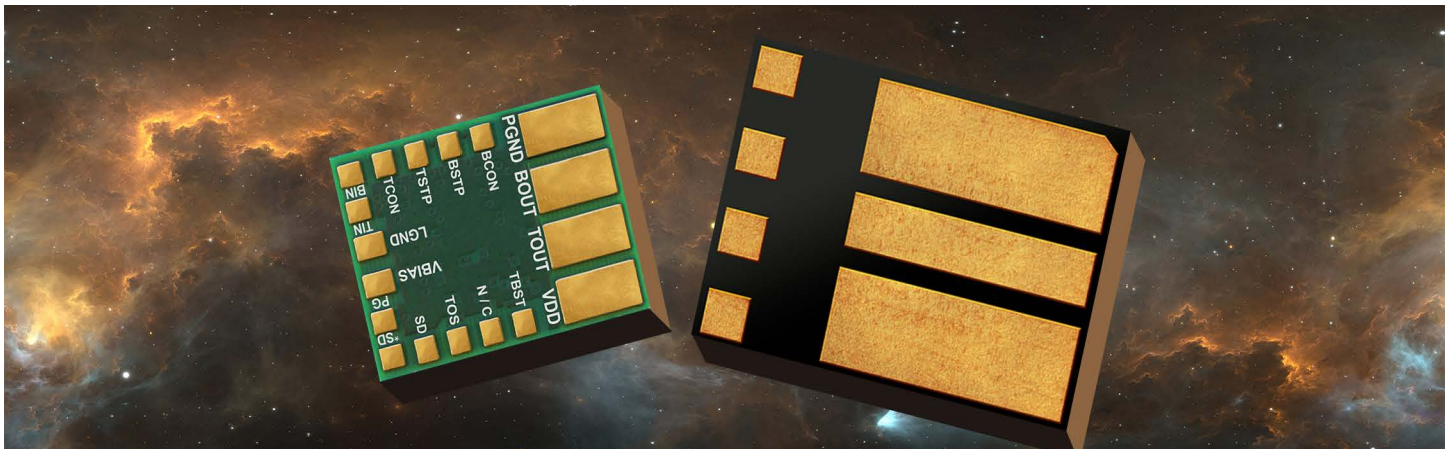
Power Supply Bypassing and Voltage Overshoot Reduction for eGaN® HEMTs



Introduction

The eGaN HEMT transistor can provide the end-user with a high-performance, reliable solution to their power switching needs. However, due to the incredible switching speeds that can be achieved by these transistors, care must be exercised in the power supply bypassing provided for the switching circuit as well as the implementation of the proper PCB layout techniques to prevent/avoid potentially-damaging voltage transients on the main power (V_{DD}) bus.

AC Bypass Capacitance Impedance vs. Frequency

An SMT capacitor used for power supply high-frequency AC current bypassing is often thought of as a purely capacitive element. However, the real-world representation of such a capacitor is a capacitor in series with a parasitic inductor in series with a parasitic resistor. The inductor arises from the physical length an area presents to the AC current flowing in it. The resistance is the amount of real impedance formed by the internal plates and connections to the capacitor when the frequency is set to the resonance point of the R-L-C circuit formed by the capacitor and its packaging parasites. The typical impedance versus frequency characteristic for a 0.1 µF, 0805-packaged SMT capacitor is shown in Figure 1.

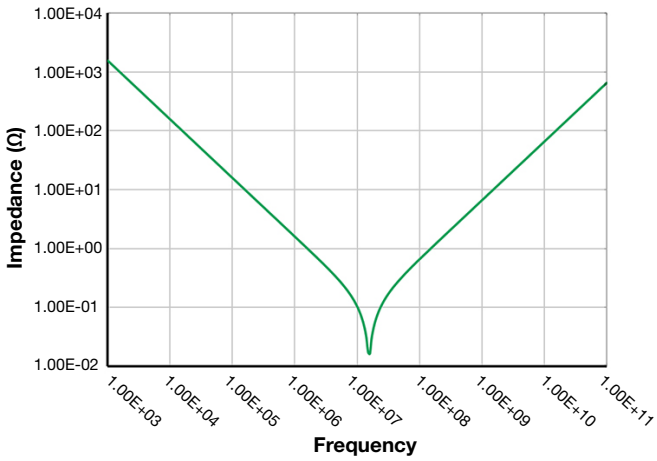


Figure 1. Impedance vs. Frequency for 0.1 µF/0805-Packaged Capacitor

As is obvious in the plot in Figure 1, to the left of the resonance frequency the capacitor's impedance is capacitive, to the right it is inductive and at resonance, it assumes the value of the ESR. Resultingly, the capacitor may be represented by the electrical model shown in Figure 2:

Figure 2. Capacitor Equivalent Circuit

Adding/paralleling multiple capacitors of the same value and size does little to change the shape of the curve shown in Figure 1. The ESR minimum point is reduced by ESR/N, where N is the number of capacitors paralleled. But the problem remains that just after the resonant frequency, the impedance becomes inductive. And instead of being a low-resistance shunt between the V_{DD} supply voltage and the return (0 V), it is an inductor whose impedance increases with increasing frequencies.

Why is this an issue? ...

Because the eGaN HEMT devices can switch ON/OFF so incredibly fast this switching comes with extremely large voltage and current slew rates, which cause associated transients. The slew rate of most interest with regards to power supply bypassing is the current slew rate, dI/dt. If an eGaN HEMT turns ON in 4 ns, carrying 25 A of drain current, then the voltage perturbation experienced just by the parasitic inductance in the 0.1 µF bypass capacitor shown in Figure 1 is:

$$V = L \cdot dI/dt,$$

Where L = 1050 pH and dI/dt = 6.25 V/ns, and

$$V = 1050 \cdot 10^{-12} \cdot 6.25 \cdot 10^{9} = 6.6\ V$$

This 6.6V peak voltage above the V_{DD} nominal level is just from the contribution of the bypass capacitor. There are other sources of inductance in the circuit, such as the induction loop inductance caused by inscribed current loop area from the V_{DD} connection to the HEMT to the ground return. As an example, consider the simple half-bridge configuration, POL power stage shown in Figure 3:

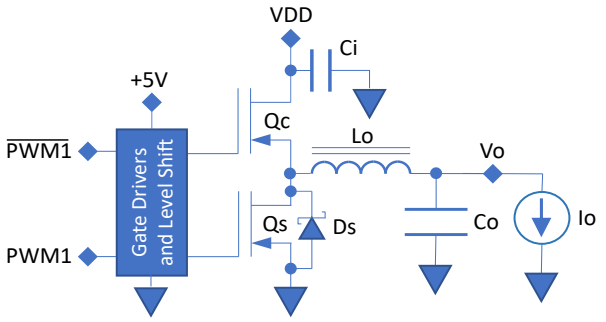


Figure 3. Half-Bridge (POL) Power Stage

High slew-rate AC current is drawn from the bypass capacitor, Ci, when switch Qs is switched OFF (current Io is interrupted in Qs, Figure 4a, a brief dead time delay is undergone (both Qc an Qs are OFF/open and diode Ds conducts, Figure 4b, and finally, switch Qc is switched ON (conducting current Io), Figure 4c.

NOTE: The current that flows in Lo is considered to be the constant value Io during the short time the switching events take place, as Lo has a value several orders of magnitude larger value than the other parasitic inductances in the circuit.

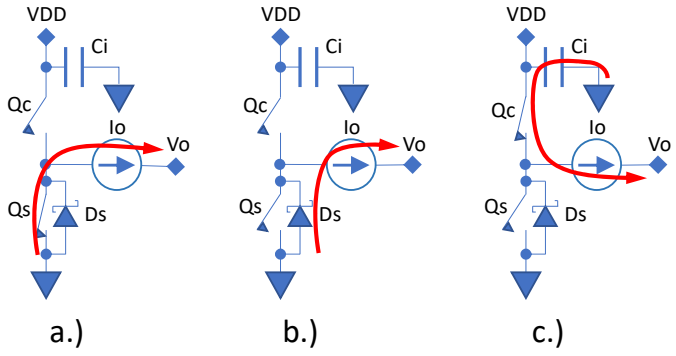


Figure 4. Half-Bridge Qs-to-Qc Switching Event

It is the last action in this chain of events, the closure (turn ON) of switch Qc, that causes high rate-of-change current to flow in capacitor Ci. And additional transient current is also caused to flow in Ci due to the output capacitance of Qs and the junction capacitance of Ds. Because the switching node (the junction of the source of Qc, the drain of Qs and the inductor, Lo) experiences a high rate-of-change of voltage when Qs turns ON, the transient current in Ct = Coss(Qs) + Cj(Ds) is given by:

$$I(Ct) = Ct \cdot V_{DD} / ton$$

For example, if Ct = 1500 pf, V_{DD} = 25 V and tr = 5 ns, then I(Ct) = 7.5 A. Thus, if Io = 25 A, a total transient current of dI = Io + I(Ct) = 25 + 7.5 = 32.5 A flows in capacitor Ci when transistor Qc is closed. The transient voltage across the parasitic inductance of Ci is given by:

$$V(Ci) = L(Ci) \cdot dI / dt,$$

Where L(Ci) is 1050 pH, dI is 32.5 A from above and dt = tr = 5ns. Thus $V(Ci) = 1050 \cdot 10^{-12} \cdot 32.5 / 5 \cdot 10^{-9} = 6.83$ V.

Remember that the above value represents the transient voltage peak from just the bypass capacitor and does not include the inductive effects of the circuit's induction loop area.

Taming Transient Voltage Overshoot With Multiple Bypass Capacitor Values

EPC Space recommends that multiple decades of bypass capacitors are utilized in order to greatly reduce or ameliorate the bypass-capacitor-induced voltage transient. For example, the composite impedance versus frequency for five capacitors in parallel: 4.7 µF/1210, 1.0 µF/1206, 0.1 µF/0805, 0.01 µF/0805 and 4700 pF/0805 is shown in Figure 5 (in **GREEN**):

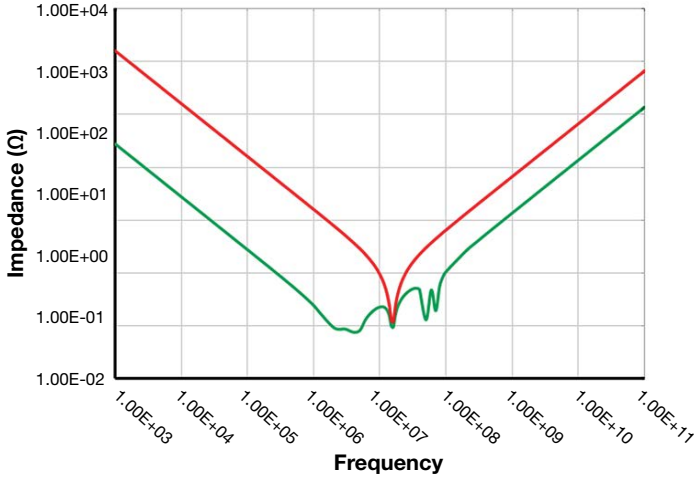


Figure 5. Composite Bypass Capacitor Impedance vs. Frequency.

The **RED** plot in Figure 5 is for a single 0.1 µF/0805 capacitor for comparison.

It can be seen that a great deal of impedance reduction can be had over a large "stopband" when utilizing multiple values of SMT capacitors in parallel.

There are two important criteria that need to be addressed such that an accurate estimation of impedance versus frequency may be made, and that the smallest possible voltage perturbation may be achieved as a result of this effort. The first is to be able to accurately estimate the inductance of the various EIA-sized SMT capacitors and the second is to recognize that it is imperative to use the smallest possible capacitor package size for each capacitor value chosen, such that the maximum voltage rating of that package is observed with regards to the V_{DD} power supply level used in the circuit.

As for the first criteria, to this end work has been done by AVX Corporation [1] to "factorize" the package inductance of the various standard-sized/dimensioned SMT capacitors. In fact, the inductance (Lc) for the various lengths and widths of associated EIA package sizes have been estimated by the following equation:

$$\mathbf{Lc = 394.727 \cdot 1.052\ L \cdot 1.317\ (L/W)},$$

where L is the length of the capacitor in EIA units (e.g. 06, 08 or 12), W is the width in the same units (e.g. 03, 05 or 10) and the resulting Lc is the package inductance in picohenries. From the AVX results it is also abundantly clear that a "broadside" capacitor (e.g. 0508 or 0612) possesses much lower inductance than it's standard-packaged counterpart (e.g. 0805 or 1206) – so the broadside style should be used wherever physically feasible and available.

All that remains for the designer is to determine the ESR value from the capacitor manufacturer, and from this the model for each capacitor chosen can be estimated and then an impedance versus frequency estimation for the paralleled capacitors, such as shown in Figure 5, may be generated.

Using the frequency bandwidth information, the designer can then estimate the frequency of the switching bandwidth for the rise time (of the high-power switching node) in the circuit from the following equation:

$$\mathbf{BW = 0.35/tr\ (Hz)}$$

If the rise time is 4 ns (from the previous example) then the bandwidth is: $0.35 / 4 \cdot 10^{-9} = 87.5$ MHz. If the composite impedance as determined previously has a null point close to this bandwidth frequency value or coincident with it, then the inductance-induced voltage perturbation has been essentially eliminated. Knowing this bandwidth value, the designer can then tailor the impedance response desired using different capacitor values and package sizes. Trial-and-error and a spreadsheet can effectively accomplish this task!

Wait. There's Something Else!

With the design/determination of the bypass capacitor values and sizes determined, there is one other task that needs to be accomplished to reduce the parasitic inductance in the circuit to as small as value as possible. This is to use the printed circuit board layout to help cancel the magnetic flux generated by the high-speed, high-current AC paths in the circuit, as illustrated in Figure 4.

The key objective in this exercise is to use adjacent PCB etch layers to create this cancellation by forcing the AC current (shown in **RED**) to flow in one direction in the top layer (where the power switch and bypass elements are mounted) and to flow in the opposite direction in the directly adjacent layer in the PCB stack-up, as shown in the example in the cross-section view of a PCB layout for the circuit shown in Figure 3, in Figure 6.

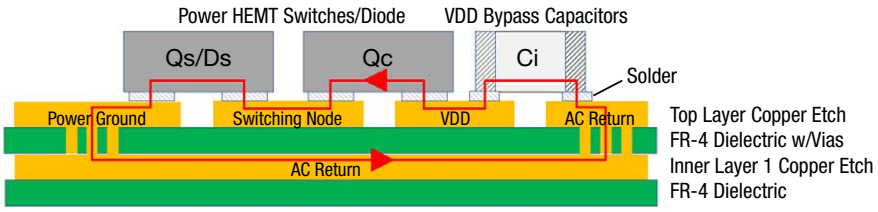


Figure 6. High-Frequency AC Current Paths in Etch (Cross-Section View)

This layer arrangement affords the closest proximity between the two etch layers and results in the best magnetic flux cancellation possible. The resultant circuit function created by the two adjacent layers acts as a one turn transformer with a dielectric core, not unlike a common-mode transformer.

Consider as an example of a component-side view of the EPC7C011 evaluation board, A board that essentially implements the circuit shown in Figure 3, as shown in Figure 7:

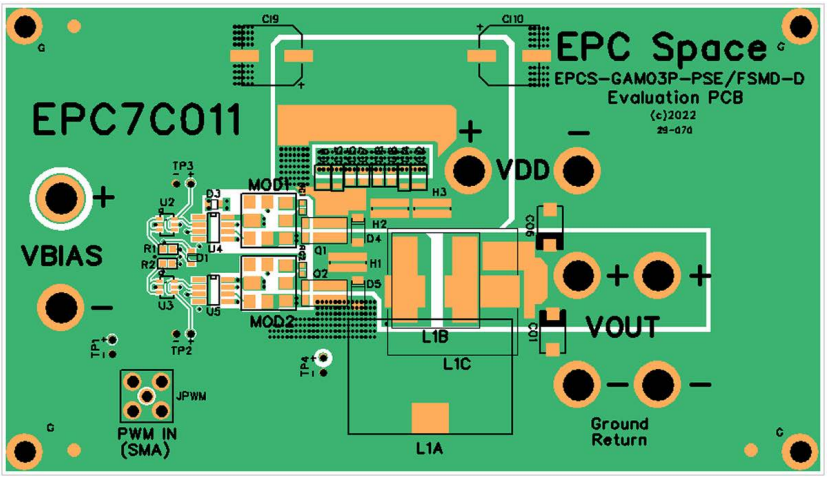


Figure 7. EPC7C011 Evaluation Board PCB Layout Example

This is a multi-function board that implements a POL power stage. Focusing in on the power stage elements in the layout results in the view as shown in Figures 8a-8c. Figure 8a shows the top side copper etch with reference designations for the area of interest, Figure 8b shows the inner layer 1 copper etch with the top layer component solder mask openings left ON to observe top-to-layer 1 alignments, and Figure 8c shows the inner layer 1 copper etch alone for clarity. The **RED** arrows indicate the direction of the high-speed AC currents in each layer.

In the layout implementation above please note the use of abundant small diameter layer-to-layer vias to reduce the inter-layer inductance. The three-sided isolation of the AC return path from the DC ground/return plane is obvious in inner layer 1 in Figure 8c.

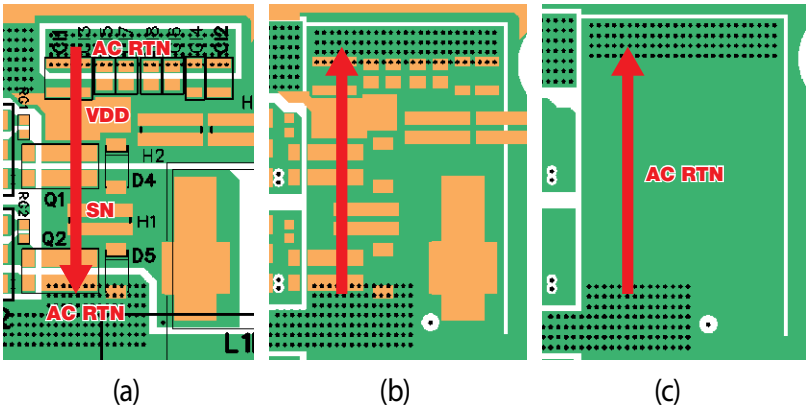


Figure 8. EPC7C011 Top and Inner Layer 1 PCB Etch Configurations for Induction Loop Current Cancellation

It should be noted that although there is never complete magnetic flux cancellation (in Figure 6 the AC current has to ascend/descend each component on the top layer but inner layer 1 is strictly planar, thus slightly shorter in travel distance, so there are minor differences in the flux path lengths of each etch layer), this technique affords the best reduction in loop inductance possible.

Well, the proof as they say is in the results, and the leading-edge switching waveform for a POL converter, with V_{DD} =25 V and Io = 10 A, that is configured as shown in Figure 3 and shares a PCB layout similar to that in Figure 8 is shown in Figure 9a and the switching node waveform is shown in Figure 9b. The rise time of the switching node as shown in Figure 9a is 6.7 ns. This value is in the typical range expected for available gate drivers and for what EPC Space considers the "optimum" PCB layout. It is obvious from the switching node waveform captured in Figure 9b that there is no discernible voltage overshoot on the leading edge (in either waveform capture), which serves as a verification of the efficacy of the recommended V_{DD} bypassing and PCB layout strategy.

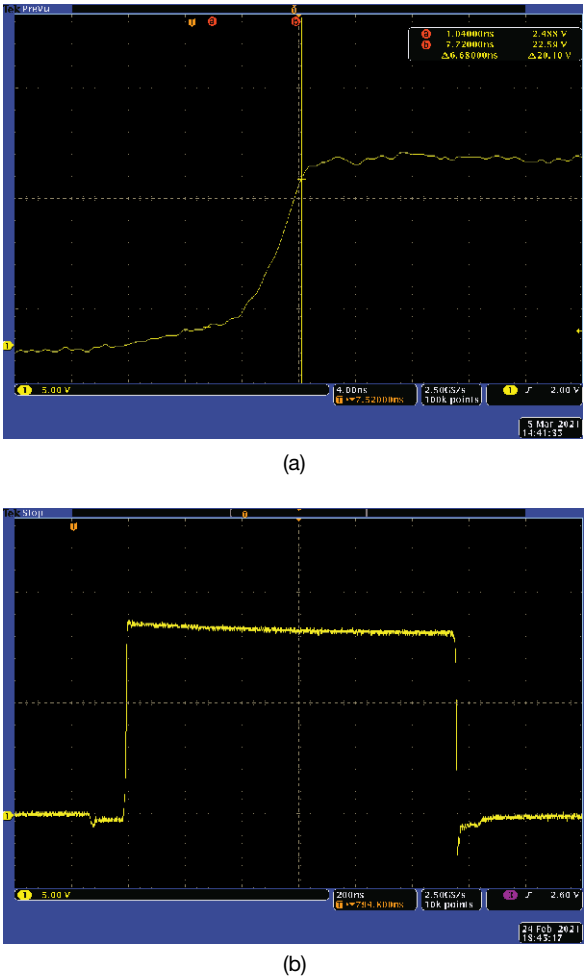


Figure 9. Rise Time and Switching Node Waveforms For Optimum V_{DD} Bypassing and PCB Layout.

Conclusion and Summary

EPC Space eGaN® Rad-Hard HEMTs have extremely fast dynamic performance which demands that special power supply (V_{DD}) bypassing and PCB layout strategies be utilized that address the detrimental effects of high-frequency parasitic elements in the power circuit. Non-ideal capacitors and induction loops both contribute parasitic inductances to the circuit. Multiple bypass capacitors of several decades of value can address the former issue, while proper PCB layout of high-frequency AC switching currents can minimize the latter.

EPC Space recommends a solution for each of the issues described previously with regards to bypass capacitors and magnetic loop induction. Several examples are shown to prove the effectiveness of the recommendations, and waveform captures are provided which show the efficacy of the recommended strategies in a real-world application circuit.

References

[1] J. Cain, *"Parasitic Inductance of Multilayer Ceramic Capacitors"*, Technical Paper, AVX Corporation, 2020.